## ABSTRACT OF THE DISCLOSURE

A metal line layout which includes two separate control spaces to address capacitive issues along speed sensitive pathways in an integrated circuit structure without negatively impacting Werner Fill processing. One control space (i.e., $DRCgap_1$) is for decreasing the spacing between various metal features to standardize such spacing, and a second control space (i.e., $DRCgap_2$) is for addressing capacitance issues along speed sensitive pathways. Between speed sensitive pathways, spacing of added metal features provided to long parallel metal lines are maintained at the second control spacing $DRCgap_2$. Spaces at the ends of such long parallel metal lines are reduced to the first control spacing $DRCgap_1$ in order to best fill three-way-intersections (TWIs) with subsequent depositions.